IXYS

Preliminary Technical Information

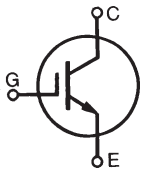
Trench Gate

IGBT

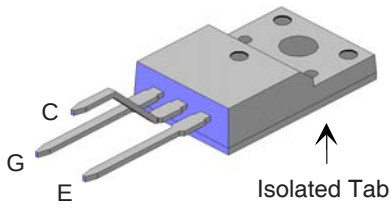
IXGP50N33TBM-A

V_{CES} = 330V
I_{CP} = 200A
$V_{CE(sat)}$ ≤ 1.6V

For PDP Applications



OVERMOLDED TO-220 W/ FORMED LEAD (IXGP...M-A)



G = Gate C = Collector
E = Emitter TAB = Isolated

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	330	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	30	A
I_{CP}	T_J ≤ 150°C, tp ≤ 10µs, duty cycle ≤ 1%	200	A
$I_{C(RMS)}$	Lead current limit	75	A
P_C	T_C = 25°C	50	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from case for 10s	300	°C
T_{SOLD}	Plastic body for 10 seconds	260	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		2.5	g

Features

- Fast switching
- Plastic overmolded tab for electrical isolation
- Low $V_{CE(sat)}$
  - for minimum on-state conduction losses

Applications

- PDP Systems
- Capacitive load circuits
- Switching power supplies

Symbol (T_J = 25°C, unless otherwise specified)	Test Conditions		Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250µA ,V_{GE} = 0V		330			V
$V_{GE(th)}$	I_C = 250µA , V_{CE} = V_{GE}		3.0		5.0	V
I_{CES}	V_{CE} = 330V				2	µA
	V_{GE} = 0V	T_J = 125°C			125	µA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V				±100	nA
$V_{CE(sat)}$	V_{GE} = 15V, I_C = 25A			1.37	1.60	V
		T_J = 125°C		1.35		V
	I_C = 50A			1.71		V
		T_J = 125°C		1.76		V

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 25A, V_{CE} = 10V, Note 1	25	42		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		1480		pF
C_{oes}			108		pF
C_{res}			15		pF
Q_g	I_C = 25A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		42		nC
Q_{ge}			9		nC
Q_{gc}			12		nC
$t_{d(on)}$	**Resistive load, T_J = 25°C**		14		ns
t_{ri}	I_C = 25A, V_{GE} = 15V		30		ns
$t_{d(off)}$	V_{CE} = 240V, R_G = 15Ω		53		ns
t_{fi}			142		ns
$t_{d(on)}$	**Resistive load, T_J = 125°C**		13		ns
t_{ri}	I_C = 25A, V_{GE} = 15V		32		ns
$t_{d(off)}$	V_{CE} = 240V, R_G = 15Ω		74		ns
t_{fi}			270		ns
R_{thJC}				2.5	°C/W

Note 1: Pulse test, t ≤ 300μs; duty cycle, d ≤ 2%.

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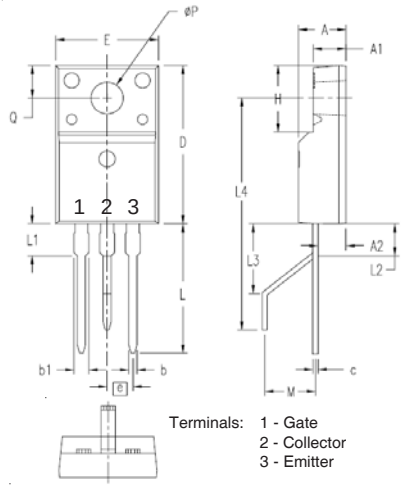

Terminals: 1 - Gate
2 - Collector
3 - Emitter

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.016	.024	0.40	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.500	.523	12.70	13.30
L1	.119	.135	3.03	3.43
L2	.098	.138	2.50	3.50
L3	.256	.295	6.50	7.50
L4	.906	.945	23.00	24.00
M	.177	.216	4.50	5.50
ØP	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ 25ºC

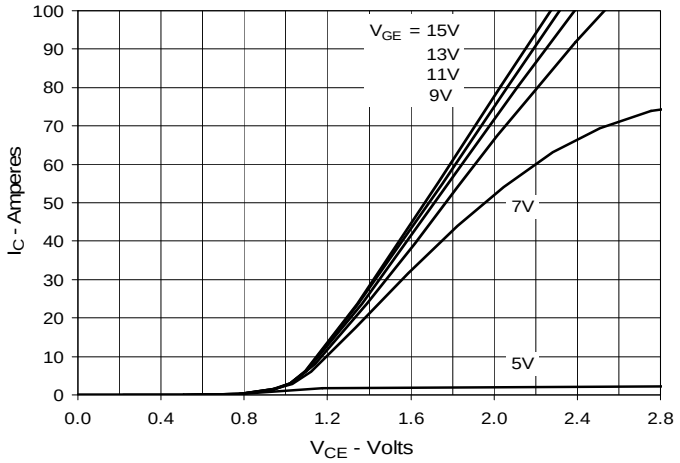

Fig. 2. Extended Output Characteristics @ 25ºC

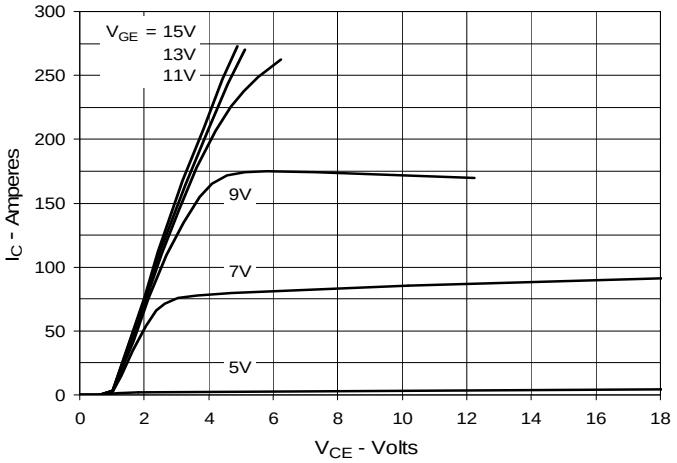

Fig. 3. Output Characteristics @ 125ºC

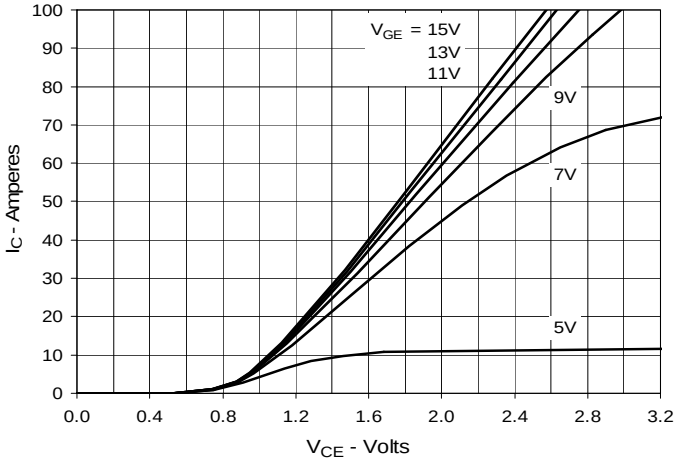

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

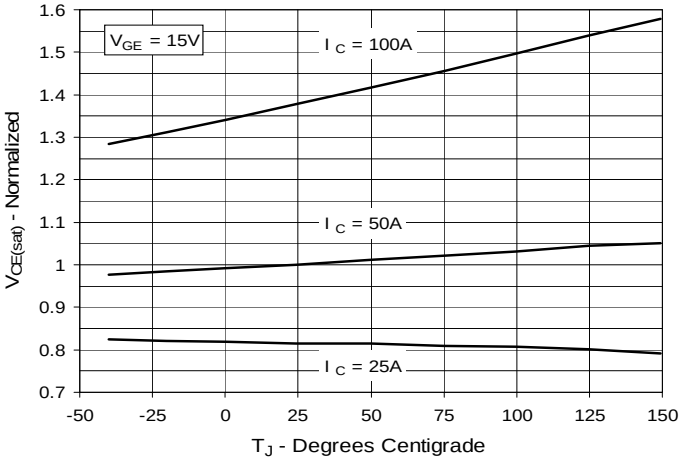

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

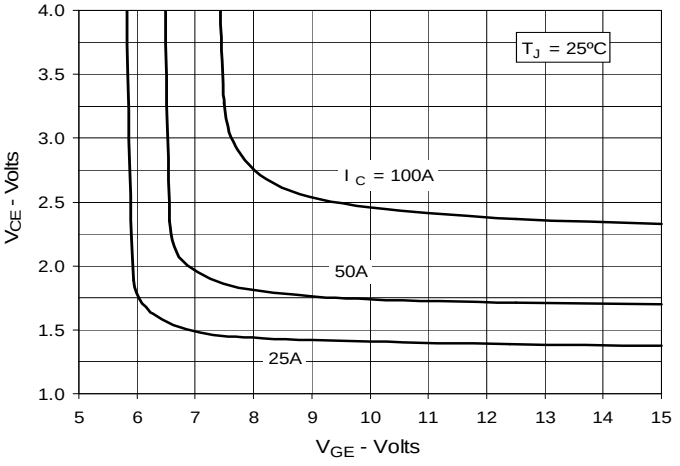

Fig. 6. Input Admittance

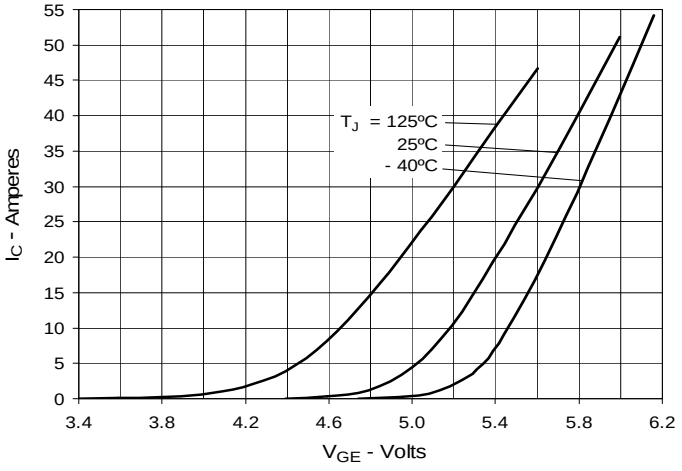

Fig. 7. Transconductance

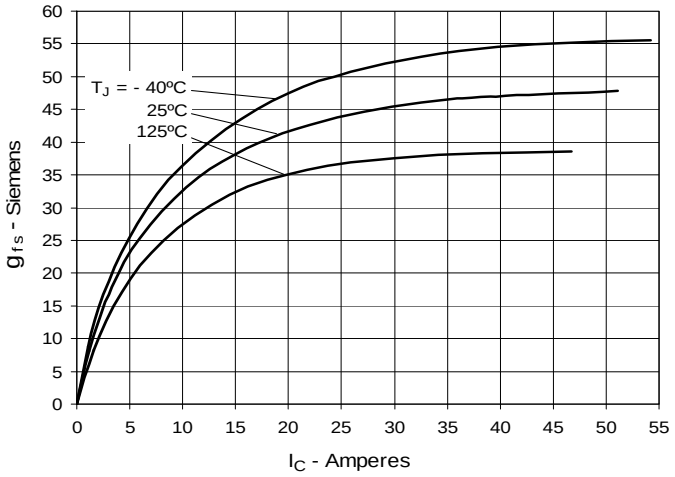

Fig. 8. Gate Charge

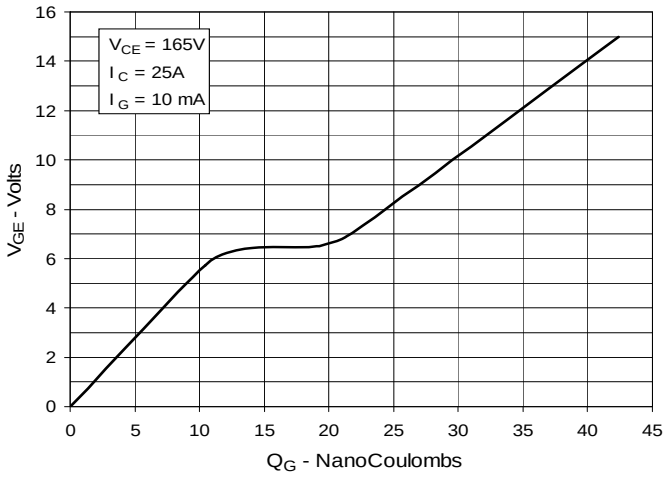

Fig. 9. Reverse-Bias Safe Operating Area

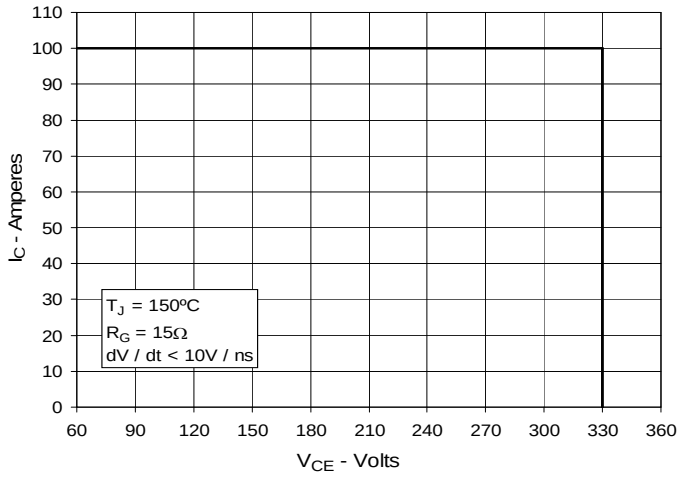

Fig. 10. Capacitance

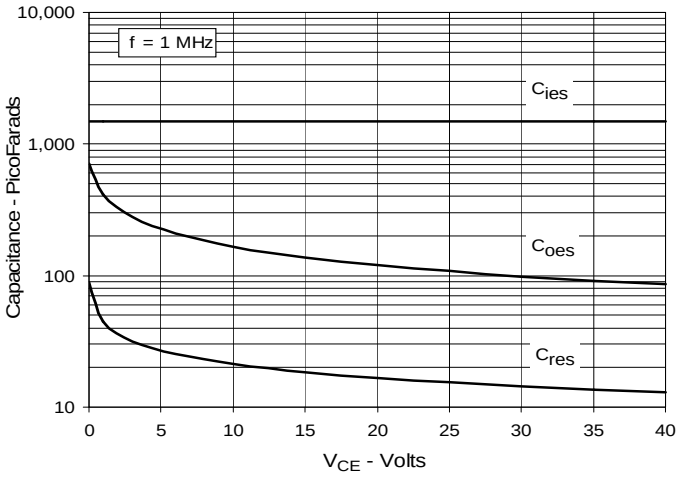

Fig. 11. Forward-Bias Safe Operating Area

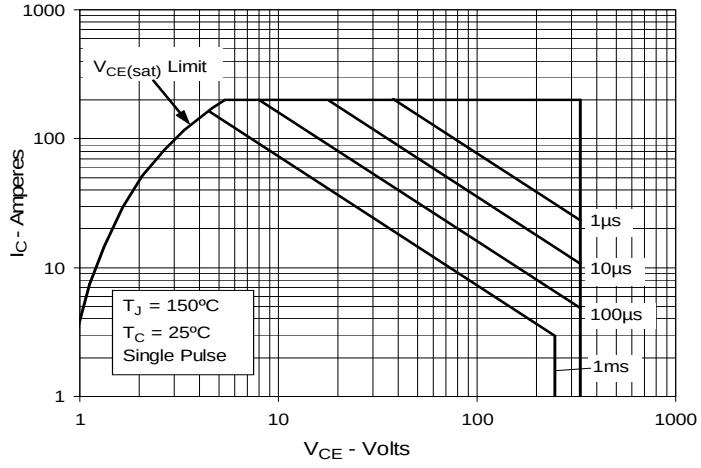

Fig. 12. Maximum Transient Thermal Impedance

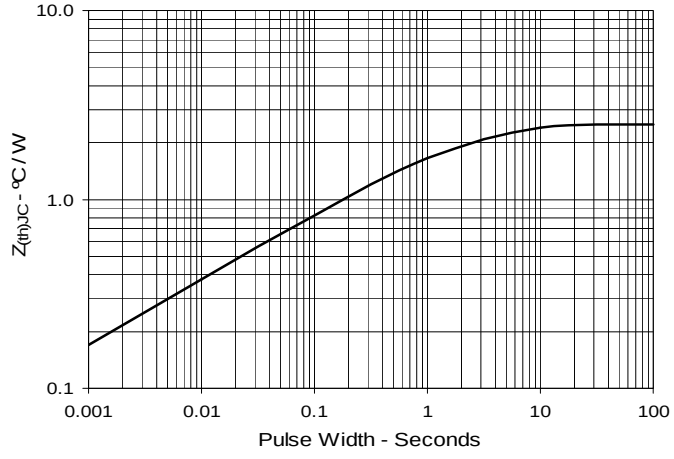

Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

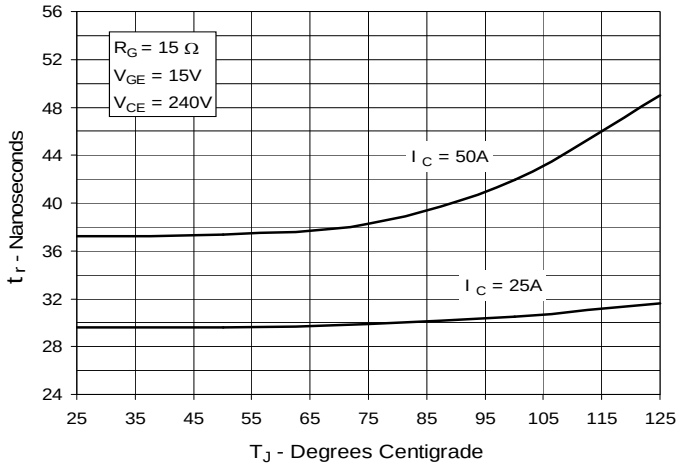

Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

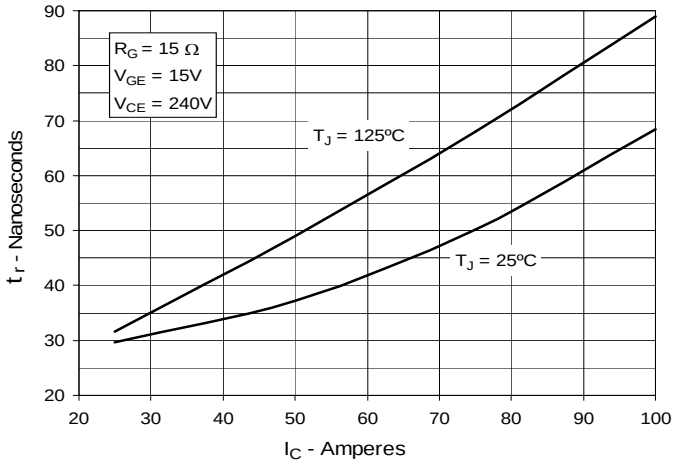

Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

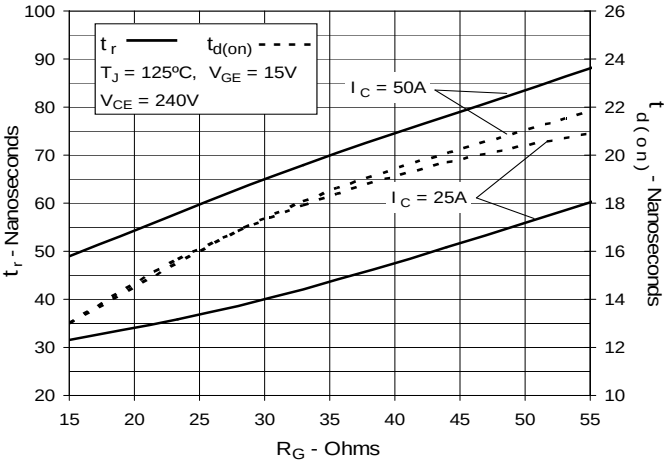

Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

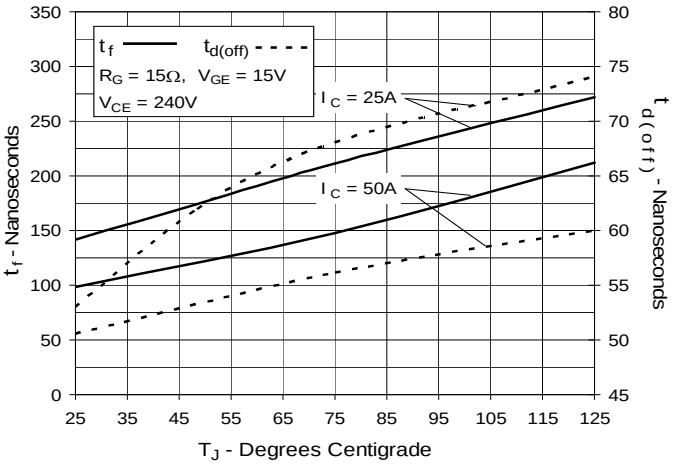

Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

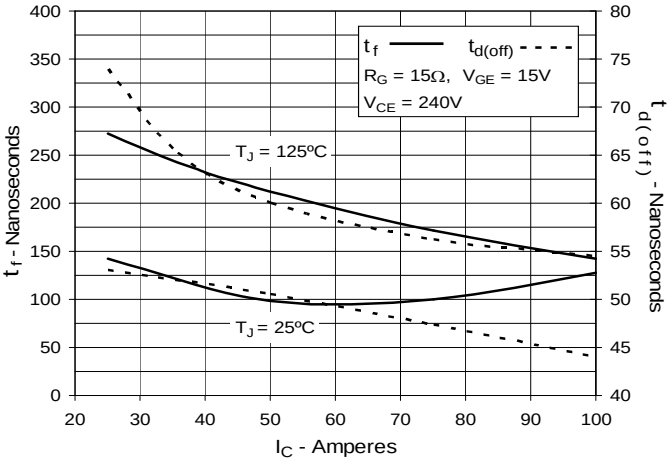

Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance